PVP 14

Code: IT4T5

II B.Tech - II Semester – Regular/Supplementary Examinations
April 2018

COMPUTER SYSTEM ARCHITECTURE
(INFORMATION TECHNOLOGY)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11 x 2 = 22

1.

a) What is memory read?
b) What is address sequencing?
c) Define control word.
d) Define virtual memory.
e) Define physical address space.
f) What is selective complement operation?
g) What is bootstrap loader?
h) What is subroutine?
i) Define page frame.
j) What is pipelining?
k) What is data transfer instruction?

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.

3 x 16 = 48 M

2.a) Draw and explain 4 bit arithmetic circuit. 8 M

b) Draw and explain bus system for four registers using multiplexers. 8 M

3.a) List out the various memory reference instructions and explain each of them with diagrams if necessary. 8 M

b) Explain about interrupt cycle with the help of flow chart. 8 M

4.a) Explain about micro instruction format and write binary program code for fetch routine. 8 M

b) Explain various addressing modes with the help of an appropriate example. 8 M

5.a) With the help of flowchart explain booth's algorithm take one numerical example you like. 8 M

b) Explain any two memory mapping methods in cache memory. 8 M

6.a) Explain about parallel priority interrupt with diagrams. 8 M

b) Explain about instruction pipelining. 8 M